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Abstract
The genetic algorithm (GA) can find an optimal solution in many complex problems. Therefore, it has been used widely in many applications. However, genetic algorithm requires very intensive computations in order to perform the optimization. Hence, a dedicated VLSI implementation for it is necessary. A flexible VLSI genetic algorithm processor is proposed in this thesis. It can perform various fitness functions dynamically to meet the requirements of various applications. Besides, various crossover operations and dynamic mutation-rate setting techniques are employed in the processor to achieve faster convergent speed. Because of the features, the proposed processor is very suitable for various real-time applications.

The proposed architecture has been verified by using Verilog HDL. Then, we employed Synopsys Design Compiler to synthesize the design with the standard-cell from TSMC's 0.35- cell library. Finally, the layout for the design was generated with the Avant! tools, Apollo (for floorplan, placement and routing), and Dracula (for DRC, ERC and LVS checks). The core size of it is about and the gate count is about 12320. In the simulation, it works with 83MHz. The hardware architecture is also implemented with an Altera FPGA chip. A demo system is built by integrating the chip with some control circuits to verify the performance of our GAP.
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